



FIG. 13 is a block diagram of a PLL circuit 1300. The circuit includes a Phase Frequency Comparing Circuit 1322, a Loop Filter 1323, a VCO 1324, a Programmable Counter 1321, a Load Pulse Generator 1325, a Frequency Dividing Circuit 1 1326-1, a Frequency Dividing Circuit 2 1327-1, and two Registers 1329 and 1328. The circuit is controlled by Reference Clock, Frequency Dividing Ratio Setting, Load Data Setting, Sync. Pulse, Phase Set, and Clock Delay Time Setting inputs. The outputs are Pixel Clock and Internal Clock.